Alternatives to the embodiments shown in Figures 2A and 2B are possible. For example, in Figure 2A the pixels are located to the right of pixels 1A and the number of source lines per pixel is reduced. However, this can be easily rearranged so that the pixels 1B are located beneath the pixels 1A as shown in Figure 2B, and reconfigured to increase the fill factor while still reducing the number of source lines per pixel. Likewise in Figure 3B, the pixels 1C are shown disposed to the right of the pixels 1A, and with dimensions selected to increase fill factor.

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In the Claims:

Please cancel claims 1-34 that are presented in the International Publication No. W0/96/31976 (corresponding to International Application No. PCT/CA92/00202) that is submitted herewith. Said claims were canceled during international stage proceedings in favor of new claims 1-34 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409) that is also submitted herewith.

Please cancel claims 3-7 and 27 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409).

Please amend claims 23 and 24 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409) as follows:

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23. (Amended) The improvement of claim 11, wherein each said thin-film-transistor (TFT) is a single gate device.

24. (Amended) The improvement of claim 11, wherein each said thin-film-transistor (TFT) is a dual gate device.

Please add new claims 35 and 36 as follows:

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35. The improvement of claim 18, wherein each said thin-film-transistor (TFT) is a single gate device.

36. The improvement of claim 18, wherein each said thin-film-transistor (TFT) is a dual gate device.